REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on July 1, 2003, and the references cited therewith.

Claims 1, 4, 8, 10-13, 16, 19 and 21 are amended, and claims 2-3, 5-7, 9, 14-15 and 17-18 are canceled; as a result, claims 1, 4, 8, 10-13, 16, 19-21 are now pending in this application.

Claim Objections

Claims 21 was objected to under 37 CFR 1.75c as being in improper form because a multiple dependent claim should refer to other claims in the alternative only

Claim 21 has been amended to be in proper form and to refer to multiple claims only in the alternative. Withdrawal of the objection to claim 21 is respectfully requested.

Specification

The Examiner stated that Figure 18 does not appear to be described in the specification. Applicant respectfully directs the Examiner's attention to the reference to Figure 18 on page 14 at line 21.

§112 Rejection of the Claims

Claims 1-21 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim 1 has been amended to more particularly point out the claimed invention and a clear definition of the phrase symmetric function has been included.

With regard to claims 2, 3, 5, 7, 9 and 17, these claims are now deleted and thus the objections of the examiner are moot.

With regard to claim 4, page 9 lines 13-23 discloses the use of EXOR elementary symmetric functions for the generation of all three of the binary outputs of a 7 to 3 parallel counter. Figure 10 illustrates a parallel counter in which the least significant bit S_0 is generated as EXOR_7_1 i.e. i=0 and hence 2^i=1. The subject of claim 4 is thus both described in its

generality and specifically with regard to the generation of the least significant bit output of the parallel counter in figure 10.

With regard to claim 8, page 9 line 24 to page 10 line 8 discloses the use of OR_7_4 for the generation of the third (N^{th}) bit S_2 i.e. N-1=2. Also figure 10 illustrates this.

With regard to claim 16, figure 17 illustrates the formation of the array of reduced maximal height. The top of the figure illustrates the formed reduced array. The reduced array comprises the prior art array as illustrated in figure 15 with the further logic combinations X, Y and Z in the array to reduce the maximal height of the array. As described in the description at page 13 line 12 to page 14 line 20, a first stage is the conventional array generation. There is then a second stage termed array deformation which comprises the implementation of the logic X, Y and Z to form the reduced array. The logic for this is illustrated in figure 18. Figure 17 only shows the reduced array since the conventional array is illustrated in figure 15.

With regard to claim 19, page 13 line 12 to page 14 line 20 described the embodiment illustrated in figures 17 and 18 which support the subject matter of claim 19.

Therefore, Applicant respectfully requests that the rejection of claim 1-21 under 35 USC 112 be withdrawn.

§102 Rejection of the Claims

Claims 1, 2, 6, 7, 10 and 13-15 were rejected under 35 USC § 102(b) as being anticipated by both Vassiliadis and Niehaus.

With regard to claims 2, 6, 7, 14 and 15, these claims have been deleted and thus the examiners objections are moot.

With regard to claims 1, 10 and 13, Niehaus does not disclose a logic circuit that includes logic for generating at least three binary outputs as elementary OR or EXOR symmetric functions of the binary inputs as now defined in the amended claims. Niehaus does not use symmetric functions for the generation of any of the outputs. In Vassiliadis only a 7 to 3 parallel counter is disclosed in which the intermediate bit C2 is not generated as an elementary OR or EXOR symmetric function of the binary inputs. There is no disclosure of the concept or principles of elementary OR or EXOR symmetric functions as discovered by the inventors and now defined in claims 1, 10 and 13. The discovery of the utility of elementary OR and EXOR

symmetric functions by the inventors allows for an efficient design of the logic for generation of intermediate output bits of not just, for example, a 7 to 3 parallel counter, but also for larger parallel counters (i.e. the primary carry bit in a 7 to 3 counter and the primary and secondary carry bits in a 15 to 4 counter). It is thus respectfully submitted that the subject matter claims of 1, 10 and 13 are neither disclosed or suggested in Niehaus or Vassiliadis.

With regard to claim 16, Chiu discloses a booth encoder and does not disclose the two stage generation of a reduced logic array prior to array reduction as claimed in claim 16. Chiu does not disclose or suggest the initial formation of logical AND combinations and a second stage of logical combination to reduce the maximal depth of the array below N bits during an array formation stage. It is therefore respectfully submitted that the objections in the Office Action regarding claim 16 have been traversed.

With regard to the prior art made of record, this is not considered to be any more pertinent to the amended claims that the prior art relied upon by the examiner.

Therefore, Applicant respectfully requests that the rejection of the claims under 35 USC 102 be withdrawn.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 349-9592) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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Date Oct. 1, 2003

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 1st day of October, 2003.

PATRICIA A. HULTMAN

Name

Signature